EXHIBIT 5

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

UNM RAINFOREST INNOVATIONS Plaintiff, v. GLOBALFOUNDRIES INC., GLOBALFOUNDRIES U.S. INC., and GLOBALFOUNDRIES U.S. 2 INC., Defendants.	CIVIL ACTION NO. 6:20-CV-243-ADA JURY TRIAL DEMANDED

Declaration of Professor Harlan Rusty Harris, Ph.D.

I, Rusty Harris, hereby declare as follows:

1. My name is Harlan Rusty Harris, and I have been retained by counsel for Plaintiff UNM Rainforest Innovations ("UNM"), formerly known as STC.UNM, to consult and provide expert opinion in support of UNM's responsive claim construction briefs submitted in conjunction with this action against GlobalFoundries. In particular, I have been asked to provide expert opinion on whether the term "growing a heteroepitaxial layer on the seed area" as used in U.S. Patent No. 9,142,400 ("the '400 Patent") would be understandable to a person of ordinary skill in the art such that it would not be indefinite under the patent laws. I have also been asked to respond to the opinion of Dr. Jeffrey Bokor, the Defendants' expert, on this issue.

2. I have personal knowledge of the facts and opinions set forth in this declaration and believe them to be true. If called upon to do so, I would testify competently thereto. I have been warned that willful false statements and the like are punishable by fine or imprisonment, or both.

3. I am being compensated for my time at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of this work. My compensation is

not contingent upon the results of my study, the substance of my opinions, or the outcome of any proceeding involving the '400 Patent. I have no financial interest in the outcome of the pending litigation or these claim construction proceedings.

4. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials, including those cited herein.

5. My analysis of the materials produced in this proceeding is ongoing, and I will continue to review any new material as it is provided. This declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

6. I received a B.S. degree in Engineering Physics with an Electrical Engineering emphasis from Texas Tech University in 1997 and an M.S. degree in Electrical Engineering from Texas Tech University in 1999. I received a Ph.D. degree in Electrical and Computer Engineering from Texas Tech University in 2003.

7. I am presently an associate professor in the Department of Electrical & Computer Engineering at Texas A&M University in College Station, Texas. My research primarily focuses on CMOS and silicon technology and materials integration. I also hold joint appointments as an Associate Professor in the Departments of Physics and Astronomy and Materials Science and Engineering at Texas A&M. I served as Assistant Professor in these departments from 2008-2014. As part of my work for the University, I teach courses in nano-scale devices and device processing, condensed matter physics and semiconductor fabrication, as well as conduct research on device science and integration, nitride-based power and RF device technology, quantum computing devices and architecture and semiconductors for detection of high energy particles.

8. Before joining the faculty at Texas A&M, I worked at Advanced Micro Devices in Austin, TX, where I managed over ten PhD-level employees as part of the Non-Planar CMOS Extension Group, which focused on the integration of FinFET and nanowire devices. Prior to AMD, I was a visiting scientist at International Sematech in Austin, TX where I studied PMOS reliability of advanced high k gate stack FET structures including NBTI, the effect of dielectric charging with metal and/or poly gates, and transient interface and thresholds degradation.

9. I am actively engaged in mentoring Ph.D. and Masters' students through internships, project management, and publications. I have mentored and served on the graduate committees of students from the University of Florida, North Carolina State University, Stanford University, the University of Texas, Texas State University, the University of North Texas, the University of California – Berkeley, the University of Central Florida, and Yale University.

10. I have over 85 articles published in peer-reviewed journals and have presented and lectured at several conferences. I have given over 20 invited talks. My publications and other qualifications are listed in my CV, which is attached as Attachment 1 to this declaration.

11. In reaching my opinions, I have reviewed the patent itself, the file history of the patent, and the parties' opening claim construction briefs and supporting materials.

12. The '400 Patent is generally directed to a semiconductor technology known as "FinFET," *i.e.*, a fin-shaped field effect transistor ("FET"). Conventional electronic devices on a semiconductor chip are typically arranged two-dimensionally, *i.e.*, laterally across the chip surface like features drawn on a map. As circuits become smaller, more complex, and more densely packed, there is less space on the chip surface to accommodate these circuit structures. Moreover, as silicon transistors have scaled to smaller and smaller dimensions, the problem of carrier confinement has emerged as a significant issue. Carrier confinement refers to the transport of

charge carriers in the channel and the ability to control this transport with voltages applied to the transistor gate. Poor carrier confinement results in leakage current, which make it difficult to turn the transistor off. Transitioning to a three-dimensional device with "fins" etched from the silicon improves such devices issues and other problems, thus allowing increased complexity, density, and miniaturization.

13. The '400 Patent claims a specific method for forming a heteroepitaxial layer. Claim 1 of the '400 Patent discloses forming a nanostructured pedestal, *i.e.*, a fin, on a semiconductor substrate, the pedestal having a top surface and a side surface. On the top surface of the pedestal is formed a seed area of about 10 to 100 nanometers in size. To form the seed area, a selective growth mask layer is placed on the top and side surface of the pedestal. The seed area is selectively exposed by removing a portion of the selective growth mask layer, and then etched back. The heteroepitaxial layer is then grown on the etched-back and exposed seed area. Figure 1 of the '400 Patent is illustrative.

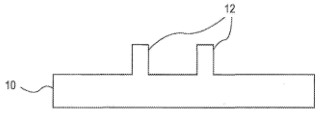

FIG. 1A

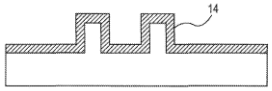

FIG. 1B

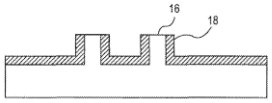

FIG. 1C

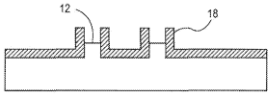

FIG. 1D

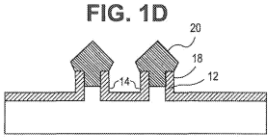

FIG. 1E

14. A primary challenge associated with the use of heteroepitaxial layers on the pedestal, or fin, involves "defects associated with the lattice and thermal expansion mismatches between the foreign material and the Si." '400 Patent at 1:64-66. In other words, defects can occur within the heteroepitaxial layer as it is grown on top of the native silicon of the pedestal. *Id*. at 1:66-2:3. The patent criticizes the use of thick buffer layers "not compatible with integration on the very small scales of today's silicon integrated circuits."

15. The '400 Patent attempts to address these short comings using seed areas with relatively small dimensions.

> Employing seed areas having relatively small dimensions in the manner disclosed herein can have one or more of the following benefits: the ability to form heteroepitaxial structures with reduced numbers of defects compared with larger area heteroepitaxial layers; the ability to form heteroepitaxial structures with zero or substantially zero defects; the ability to form heteroepitaxial pillar structures that are flexible and/or that can accommodate strain better than heteroepitaxial layers grown on a planar substrate surface; or the ability to form small area heteroepitaxial films that can accommodate strain better than heteroepitaxial layers grown on a large area of a substrate surface.

Id. at 3:61-4:5. The patent also states that "[w]hen the dimensions of a growth area are reduced to below the average scale to nucleate a defect such as a threading dislocation, it is possible to grow heterogeneous materials without nucleating either threading dislocations or antisite defects (boundaries where two grains of the zinc-blende III-V crystal are misoriented by 180°)." *Id*. at 4:14-19.

16. Claim 1 of the '400 Patent states:

> 1. A method for making a heteroepitaxial layer, the method comprising:
>
> [a] providing a semiconductor substrate;
>
> [b] forming a nanostructured pedestal on the semiconductor substrate, the pedestal having a top surface and a side surface, the top surface forming a seed area having a linear surface dimension that ranges from about 10 nm to about 100 nm;

[c] providing a selective growth mask layer on the top surface and side surface of the pedestal;

[d] removing a portion of the selective growth mask layer to expose the seed area of the pedestal;

[e] selectively etching back the exposed top surface of the pedestal; and

[f] growing a heteroepitaxial layer on the seed area.

17. I understand that the parties agreed that the term "seed area" carries its plain and ordinary meaning, which the Court has said is "the area on which the epitaxial growth could occur."

18. I understand that Defendants and Dr. Bokor contend that claim 1 of the '400 Patent cannot be performed as drafted. I understand that Defendants argue that a heteroepitaxial layer cannot be grown on the "seed area" because the "seed area no longer exists because it was removed by the "selectively etching back…" step. In support of their position, Defendants provide this annotated version of Figure 1D, which according to Defendants and their expert, show that the "seed area" is limited to the red highlight and has been removed by the etching back step.

19. I disagree with Defendants' and Dr. Bokor's position and their reading of the claim language. A person of ordinary skill in the art would not understand that the "seed area" no longer exists or was removed by virtue of the "selectively etching back" step. This interpretation of the claims is inconsistent with the straight-forward claim language and the specification. This reading of the claim language is especially erroneous given the importance of the "seed area" to the benefits of the claimed invention as set forth in the specification in columns 3 and 4.

20. Under the claim language, after a portion of the selective growth mask layer is removed to expose the seed area, a heteroepitaxial layer is grown on the seed area. I understand that Defendants and their expert believe that further etching back of the top surface of the pedestal after the seed area has been exposed results in the removal of the "seed area." This makes no sense.

The "seed area" is not removed. The seed area does not disappear. The seed area continues to exist, albeit at a new level, after etching back. This is consistent with the Court's guidance that a "seed area" is "the area on which the epitaxial growth could occur." Epitaxial growth could occur at either location. A person of ordinary skill in the art would consider the "seed area" to be on the top surface of the pedestal—even after a selective etch back—and having a linear surface dimension that ranges from about 10 nm to about 100 nm, as reflected in the second recited claim step. *Id*. The specification explains this in connection with its description of both Figures 1 and 2. '400 Patent at 5:64-6:6; 7:23-33

21. A skilled artisan would not understand that the "seed area" exposed has suddenly disappeared because of the etch back. It is important to understand how a POSITA would view the material that is comprised in the fin (or "pedestal" as the specification calls it), the top surface of which is the seed layer. Because a heteroepitaxial layer is a continuation of the crystal within the fin, albeit with a different crystalline material, a POSITA engaged in implementing heteroepitaxy would look at the fin crystallographically. In modern semiconductor device fabrication, the fin crystal is a spatially near-perfect repetitive ensemble of atoms bound to each other. Furthermore, all semiconductors used in the formation of fins (including silicon, the most ubiquitous) are highly symmetric such that every atomic layer would appear identical to the one above or below it.

22. Since a POSITA views the fin and heteroepitaxial layer in terms of their crystal properties, and inherently knows that any atomic surface atop the fin, assuming appropriate cleanliness, is suitable for epitaxial processing, then altering the height of the fin as described in '400 would still result in a seed area on the top surface of the fin. Contrary to the view of Defendants and their expert, a person of ordinary skill in the art would know precisely where the epitaxial growth would occur in the final step. There is no ambiguity. There is no confusion.

23. In fact, a POSITA would find the notion that one has "lost" the seed area due to etching completely and fundamentally inconsistent with the nature of epitaxial processing. To further underscore this perception, regardless of whether the fin is left in its original state or undergoes the "selectively etching back" step, prior to introducing the wafer to heteroepitaxy, the surface has to be cleaned and prepared for epitaxial processing. This typically consists of exposing the wafer to several solution that (1) strip carbon and other impurities from the surface, (2) mildly oxidizes a few monolayers of silicon atoms at the surface, and then (3) etches this silicon oxide away to leave a pristine seed area primed and ready for epitaxial processing. This surface preparation process is required and well known, and it already removes the exact portion of the top of the fin that the Defendants and their expert indicate in the annotated Fig. 1D. Therefore, to argue that a person of ordinary skill in the art would blindly rely on the claim's use of a "definite article" in fact defies what a skilled artisan would readily understand and would very likely implement as part of heteroepitaxial growth.

24. I respectfully note that Dr. Bokor's conclusory declaration does not grapple with this and does not reconcile from a technical standpoint his opinion that the "seed area" is removed with the fundamentals of semiconductor manufacturing explained above. Dr. Bokor certainly has not subjected his view to any technical rigor or applied any method that would be accepted in the field. His position seems to be predicated on a distorted reading of the claims and not a scientific analysis of the claims, the specification, the inventors' goals, or the benefits of the invention. Thus, there is nothing in his declaration that warrants a specific response. Should he update his declaration with a more technical challenge to the claims, I will respond accordingly.

25. Finally, I understand that Defendants argue that the claim must be redrafted in order to convey this common-sense meaning. I disagree. The claim as drafted is straightforward and

easily understood by the skilled artisan, especially in light of the specification, with reasonable certainty.

I declare under penalty of perjury that the foregoing is true and accurate to the best of my knowledge.

Executed on September 25th, 2020 in College Station, Texas.

H. Rusty Harris, Ph.D.